

INTERFERENCE INITIAL MEMORANDUM

Count # 1

To the Board of Patent Appeals and Interferences:

An interference is proposed involving the following 2 parties

PARTY SAKAGUCHI et al.	APPLICATION NO. 09/161,774	FILING DATE 29 September 1998	PATENT NO., IF ANY NONE	ISSUE DATE, IF ANY NONE
If the involved case is a patent, have its maintenance fees been paid? <input type="checkbox"/> Yes <input type="checkbox"/> No <input checked="" type="checkbox"/> Not due yet				
Proposed priority benefit (list all intervening applications necessary for continuity):				
COUNTRY	APPLICATION NO.	FILING DATE	PATENT NO., IF ANY	ISSUE DATE, IF ANY
US	08/863,717	27 May 1997	5,856,229	15 January 1999
US	08/401,237	09 March 1995	NONE	
Japan	7-045441	06 March 1995		
Japan	6-039389	10 March 1994		
The claim(s) of this party corresponding to this count:				
PATENTED OR PATENTABLE PENDING CLAIMS 97-104			UNPATENTABLE PENDING CLAIMS None	
The claim(s) of this party NOT corresponding to this count:				
PATENTED OR PATENTABLE PENDING CLAIMS None			UNPATENTABLE PENDING CLAIMS None	
PARTY MATSUSHITA et al.	APPLICATION NO. 08/595,382	FILING DATE 01 February 1996	PATENT NO., IF ANY 5,811,348	ISSUE DATE, IF ANY 22 September 1998
If the involved case is a patent, have its maintenance fees been paid? <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No <input type="checkbox"/> Not due yet				
Proposed priority benefit (list all intervening applications necessary for continuity):				
COUNTRY	APPLICATION NO.	FILING DATE	PATENT NO., IF ANY	ISSUE DATE, IF ANY
NONE				
The claim(s) of this party corresponding to this count:				
PATENTED OR PATENTABLE PENDING CLAIMS 1 - 11			UNPATENTABLE PENDING CLAIMS NONE	
The claim(s) of this party NOT corresponding to this count:				
PATENTED OR PATENTABLE PENDING CLAIMS 8			UNPATENTABLE PENDING CLAIMS	
(Check off each step, if applicable) INSTRUCTIONS				
<input checked="" type="checkbox"/> 1. Obtain all files listed above. <input checked="" type="checkbox"/> 2. Confirm that the proposed involved claims are still active and all corrections and entered amendments have been considered. The patents must not be expired for, among other things, failure to pay a maintenance fee (Check PALM screen 2970). <input checked="" type="checkbox"/> 3. If one of the involved files is a published application or a patent, check for compliance with 35 U.S.C. 135(b). <input checked="" type="checkbox"/> 4. Obtain a certified copy of any foreign benefit documents where necessary (37 CFR 1.55(a)). <input checked="" type="checkbox"/> 5. Discuss the proposed interference with an Interference Practice Specialist in your Technology Center.				
DATE 14 July 2004	PRIMARY EXAMINER (Signature)		ART UNIT 2823	TELEPHONE NO. 703-308-7502
DATE	INTERFERENCE PRACTICE SPECIALIST or TECHNOLOGY CENTER DIRECTOR (signature) <i>Hrenkay Khan</i>			TELEPHONE NO. 571 272 - 1606

Count

Claim 97 of U.S. Application S.N. 09/161,774

Or

Claim 1 of U.S. Patent 5,811,348 to Matsushita et al

Claims Corresponding to the Count

Why claims 97-104 of Application S.N. 08/161,774 correspond to the count:

Claim 97 corresponds exactly to the count.

Claim 98 adds to the count the limitation that the substrate is silicon which feature is obvious in view of the count and Sato (Extended Abstracts, Electrochemical Society, Vol. 94-1 (1994), pp.705-6, copy attached at tab B of the attachment which shows formation of a porous layer on a Si substrate. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sato to enable formation of a porous semiconductor layer.

Claim 99 adds to the count the limitation that the porous layer is a silicon layer which is obvious in view of the count and Sakaguchi et al U.S. Patent 5,277,748 (of record) which shows formation of a porous layer on a silicon substrate. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable provision of the substrate of the count.

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Claim 100 adds to the count in requiring a further step of oxidizing the porous layer after it is formed which is obvious in view of the count and U.S. Patent No. 5,277,748 which shows oxidizing a porous layer. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable formation of a bonding layer.

Claim 101 adds to the count in requiring oxidizing the porous silicon layer at a temperature of 400°C which is obvious in view of the count and U.S. Patent No. 5,277,748 which shows oxidation of porous Si at 400°C. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable the oxidation step to be performed in formation of a bonding layer.

Claim 102 adds to the count in requiring oxidizing the porous layer which is obvious in view of the count and U.S. Patent No. 5,277,748 which shows oxidizing a porous layer. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable formation of a bonding layer.

Claim 103 adds to the count in requiring slightly etching an end face of the porous layer which is obvious in view of the count and Sakaguchi '748 which shows selective etching of a porous layer. In view of the disclosure therein that the porous layer is removed it would have been within the scope of one of ordinary skill in the art to remove a portion of the porous layer prior to the splitting step.

Claim 104 adds to the count in forming the semiconductor layer by epitaxial growth using CVD which feature is obvious in view of the count and Sakaguchi '748 which shows epitaxial growth of a semiconductor layer by CVD. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable formation of the semiconductor layer.

Why claims 1-7 and 9-11 of Matsushita et al (U.S. Patent 5,811,348) correspond to the count

Claim 1 corresponds exactly to the count.

Claim 2 adds to the count the limitation that the substrate is silicon which feature is obvious in view of the count and Sato (Extended Abstracts, Electrochemical Society, Vol. 94-1 (1994), pp.705-6, copy attached at tab B of the attachment which shows formation of a porous layer on a Si substrate. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sato to enable formation of a porous semiconductor layer.

Claim 3 adds to the count the limitation that the porous layer is a silicon layer which is obvious in view of the count and Sakaguchi et al U.S. Patent 5,277,748 (of record) which shows formation of a porous layer on a silicon substrate. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable provision of the substrate of the count.

Claim 4 adds to the count in requiring a further step of oxidizing the porous layer after it is formed which is obvious in view of the count and U.S. Patent No. 5,277,748 which shows oxidizing a porous layer. It would

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have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable formation of a bonding layer.

Claim 5 adds to the count in requiring oxidizing the porous layer at a temperature of 400-600°C which is obvious in view of the count and U.S. Patent No. 5,277,748 which shows oxidation of porous Si at 400°C. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable the oxidation step to be performed in formation of a bonding layer.

Claim 6 adds to the count in requiring H₂ –annealing of the porous layer which is obvious in view of the count and Sato which shows baking the porous layer in H₂ at 900-1040°C. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sato to reduce the quantity of defects as disclosed by Sato.

Claim 7 adds to the count in requiring H₂ –annealing of the porous layer at 950-1000°C which is obvious in view of the count and Sato which shows baking the porous layer in H₂ at 900-1040°C. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sato to reduce the quantity of defects as disclosed by Sato.

Claim 9 adds to the count in requiring H₂ –annealing of the porous layer which is obvious in view of the count and Sato which shows baking the porous layer in H₂ at 900-1040°C. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sato to reduce the quantity of defects as disclosed by Sato.

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Claim 10 adds to the count in requiring a further step of oxidizing the porous layer after it is formed which is obvious in view of the count and U.S. Patent No. 5,277,748 which shows oxidizing a porous layer. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the count and Sakaguchi '748 to enable formation of a bonding layer.

Claim 11 corresponds to the count in that it merely labels the semiconductor layer as a "plurality of layers" which characterization is applicable to any layer. Alternatively, it would have been within the scope of one of ordinary skill in the art to combine the teachings of U.S. Patent 4,727,047 of forming more than 1 semiconductor layer in formation of a solar cell and the count to enable formation of a solar cell.

Why claim 8 of Matsushita et al (U.S. Patent 5,811,348) does not correspond to the count:

Claim 8 requires forming an oxide film on the entire structure after forming the porous layer and removing the oxide layer to form a wedge-shaped gap in an interface between said porous layer and said semiconductor layer which is neither found in the count nor disclosed or suggested by the prior art taken alone or in combination.

35.C10530C/D2



PATENT APPLICATION

Free
Amdt
B
10/27/99
A. Jenkins

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

KIYOFUMI SAKAGUCHI, ET AL.

Application No.: 09/161,774

Filed: September 29, 1998

For: PROCESS FOR PRODUCTION
OF SEMICONDUCTOR
SUBSTRATE

)
: Examiner: Not Yet Assigned

)
: Group Art Unit: ~~2812~~ 2823

)
: September 22, 1999

Assistant Commissioner for Patents
Washington, D.C. 20231

SECOND PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits, please further
amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel Claims 22 - 96 without prejudice to
or disclaimer of the subject matter recited therein.

Please add new Claims 97 through 104 as follows:

97. A method for separating a semiconductor layer
from a substrate, comprising:

forming a porous layer on a surface of a
substrate by an anodic oxidization;

forming at least one semiconductor layer on said porous layer; and

separating said semiconductor layer from said substrate by forming a mechanical rupture in said porous layer.

A 98. A method for separating a semiconductor layer from a substrate according to claim ⁹⁷~~17~~, wherein said substrate is a Si substrate.

B 99. A method for separating a semiconductor layer from a substrate according to claim ⁹⁷~~17~~, wherein said porous layer is a Si porous layer.

B 100. A method for separating a semiconductor layer from a substrate according to claim ⁹⁷~~17~~, wherein the method further comprises a step of oxidizing said porous layer after forming said porous layer.

B 101. A method for separating a semiconductor layer from a substrate according to claim ¹⁰⁰~~17~~, wherein said porous layer is oxidized at a temperature of 400°.

102. A method for separating a semiconductor layer from a substrate comprising:

forming a porous layer on a surface of a substrate;

oxidizing said porous layer;

forming at least one semiconductor layer on said porous layer;

separating said semiconductor layer from said substrate by forming a mechanical rupture within said porous layer.

C 103. The method for separating a semiconductor layer from a substrate according to ^{Claim} 97 or 102 wherein the method further comprises slightly etching an end face of the porous layer to facilitate the subsequent separation of the semiconductor layer from the substrate.

104. A method according to Claim 97, wherein said at least one semiconductor layer is formed by epitaxial growth using Chemical Vapor Deposition.

REMARKS

Claims 97-104 are now pending. Previously pending claims 22-96, which had been added in the Preliminary Amendment filed September 29, 1999, have been canceled without prejudice or disclaimer of subject matter. Claims 97 and 102 are the independent claims. Claims 97-102 have been copied from U.S. Patent No. 5,811,348, copy attached at TAB A, which issued September 22, 1998.

Applicants wish to personally interview the Examiner in this case before any action on the merits. Accordingly, before taking up this application, the Examiner is kindly requested to contact the undersigned attorney to